High-Thermal-Conductivity (1.0 W/(m·K)) Dry-Film Solder Resist at 20 µm : Compatible with Standard Process Flow and Steady-State Thermal Validation

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***Abstract*— Compact AI/edge modules increasingly rely on heat conduction through package stack, where solder resist (SR) can become a thermal bottleneck. We report a photosensitive dry-film high-thermal-conductivity solder resist (HTCSR) engineered for IC-substrate integration that delivers isotropic thermal conductivity of 1.2 W/(m·K) at a thickness of 20 µm (≈5 × that of a conventional package SR, ~0.2 W/(m·K)) while remaining compatible with a standard lamination–exposure–alkaline development–thermal cure workflow. The HTCSR exhibits a melt-viscosity profile comparable to a conventional packaging grade SRs up to 120 °C, void-free gap filling on copper patterns (L/S = 20/20 µm), low cured-surface roughness and 100-µm opening patternability. Insulation reliability under b-HAST (130 °C/85%RH/5 V, 200 h) remains comparable to the reference SR, maintaining insulation resistance > 1.0 × 10^6 Ω. In steady-state thermal tests using a controlled heater/cold-plate fixture, replacing only the SR with HTCSR (k=1.0 W/(m·K)) reduced the equilibrium temperature by 41 °C at 5 W relative to a general SR, corroborated by IR thermography indicating enhanced lateral heat spreading and a reduced through-plane thermal gradient across the SR layer. These results demonstrate a practical, process-compatible route to thinner, thermally managed substrates without sacrificing patternability and insulation reliability.**

Keywords*— *Thermal management, Advanced packaging, Solder resist, Steady-state Thermal Validation, High insulation reliability, High planarity, Embeddability.

I. Introduction

As AI-enabled perception and edge computing become more widespread, demand is rising for high-density electronic modules where conventional thermal solutions (e.g., heat sinks; Fig. 1) are impractical due to form-factor and integration constraints [1-2]. In such compact packages, heat must be conducted through the package stack, and thermal dissipation often depends on contacting dielectric materials [3]. Elevated junction temperatures broadly degrade performance and reliability (e.g., increased leakage, noise, timing margins), so lowering thermal resistance within the package is essential. However, conventional solder resists (SRs) have been optimized for electrical insulation, chemical resistance, and fine patterning, rather than device level thermal management [4]. While die-backside heat extraction has been widely studied, systematic evaluations that leverage substrate-side materials remain limited [5-8]. In architectures where the die front side cannot host a heat sink—for example, optics-constrained image modules such as CIS—the substrate becomes the primary heat-extraction path, highlighting the importance of substrate materials.

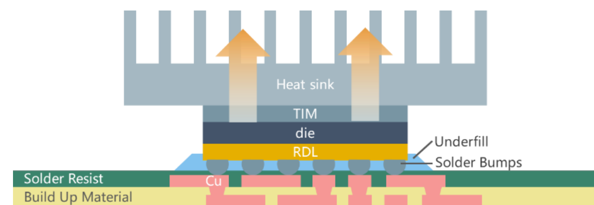

Fig. 1 Schematic drawing of conventional solution for heat generation from IC chip.

Previously, chip-temperature reduction has been reported by inserting a thermal spreading layer between the build-up dielectric and the SR (e.g., a 25 µm graphite sheet with a 20 µm adhesive layer), but this requires additional lamination/laser processes and increases total thickness and the risk of electrical short circuits [9]. On the other hand, research on the thermal conductivity of solder resist has been limited to PCB applications [10], and no theoretical experiments or practical examples regarding the thermal conductivity of solder resist for packaging have been reported.

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DOI 10.1109/ECTC51846.2026.00119

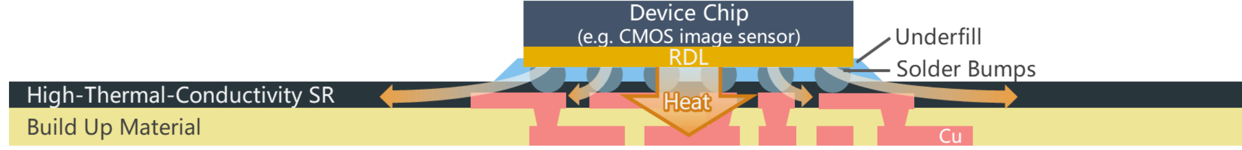

Fig. 2 Schematic drawing of thermal spreading through High-thermal-conductivity SR layer.

To address these gaps, we develop and evaluate a high–thermal-conductivity photosensitive dry-film SR (HTCSR) formulated for IC-substrate fabrication (Fig. 2). Target specifications include thermal conductivity, $k \geq 1.0$ W/(m·K) at a thickness of 20 μm (approximately five times that of conventional package-use SRs with $k \approx 0.2$ W/(m·K)), compatibility with the standard substrate fabrication processes and chemicals, such as standard lamination–exposure–alkaline development–thermal cure flow, support 100 μm aperture patterning, and provide the surface smoothness suitable for package substrates. We systematically characterize melt viscosity vs. temperature for process compatibility, embeddability and gap filling over 20/20 μm Cu pattern, surface planarity/roughness, and insulation reliability via biased highly accelerated temperature and humidity stress test (b-HAST) (130 °C/85%RH/5 V, 200 hr). We then quantify steady-state thermal performance using a controlled heater/heat-sink fixture with IR thermography and temperature sensing, isolating the impact of SR replacement only on equilibrium temperature under fixed power dissipation. This study demonstrates that substrate-side thermal mitigation is achievable without altering baseline substrate fabrication flows and provides clear, quantitative evidence of temperature reduction attributable to the SR layer itself.

At 20 μm thickness, it may serve the same purpose while also supporting module thinning.

II. Experimental Section

A. Process Compatibility Assessments as a solder resist

Firstly, the process compatibility of high-thermal-conductivity SR was evaluated with the melt viscosity value of the dry film, the developing test and the embeddability test on the substrates.

The test sample for measuring the melt viscosity of the HTCSR was prepared by repeated lamination of the dry film by a roll laminator (TAISEI LAMINATOR, VA-770) until a total thickness of 200 μm was obtained. Then, their melt viscosity values were measured by a rheometer (Thermo Scientific HAAKE, RheoStress 6000).

In order to confirm the resolution performance of the HTCSRs, dry film HTCSRs of 20 μm thickness were vacuum laminated on copper clad laminate (CCL). After the lamination, the HTCSRs were exposed to 50 – 250 mJ/cm^2 of UV light (365 nm) with an exposure machine (ORC, Mms504D). Then, the HTCSRs were developed with 1.0 wt% Na_2CO_3aq. After that, HTCSRs were exposed to 1000 mJ/cm^2 as a post UV process and then heated at 160 °C for 60 min for heat curing. The via was observed using a scanning electron microscope (SEM).

The embeddability was confirmed by vacuum lamination of HTCSRs on a substrate with a pattern of L/S = 20/20 μm. After that, HTCSRs were exposed to 1000 mJ/cm^2 as a post-UV process and then heated at 160 °C for 60 min for thermal curing. Then, the cross section of the substrate with the HTCSR laminated on the pattern was observed using SEM.

B. Thermal Characterization

The thermal conductivity values listed below were calculated from (1) using the measured values of the specific heat capacity, density and thermal diffusivity.

$$K = \rho \cdot C_p \cdot \alpha \quad (1)$$

Here, K is the thermal conductivity of the material (W/(m・K)), ρ is the mass density (kg/m^3), C_p is the specific heat capacity at constant pressure (J/(kg・K)) and α is the thermal diffusivity (m^2/s). The consistency of the units can be verified as follows:

$$(\rho)\cdot(C_p)\cdot(\alpha) = (\mathrm{kg/m^3})\cdot(\mathrm{J/(kg \cdot K)})\cdot(\mathrm{m^2/s}) = (\mathrm{J/(s \cdot m \cdot K)}) = (\mathrm{W/(m \cdot K)}) \quad (2)$$

This corresponds to the SI unit of thermal conductivity.

For measurement of the specific heat capacity, density and thermal diffusivity, a 20-μm-thick dry-film HTCSR was repeatedly laminated onto a copper foil and exposed to UV light at 1000 mJ/cm² (365 nm), with the lamination and exposure steps alternated 10 times, and then cured at 160 °C for 60 min. Finally, the sample for measurement was obtained by peeling off from the copper foil. The specific heat capacity was measured by DSC (TA Instruments, DSC Q100). The density value was determined by an electronic densimeter (Alfa Mirage, SD-200L). The value of the thermal diffusivity was measured by periodic heating method thermal diffusivity measurement system (ADVANCE RIKO, FTC-RT).

For experimental validation, a steady-state thermal test fixture was constructed, in which the sample was clamped between a water-cooled copper heat sink and a constant-power

copper coil heater. Thermal-equilibrium temperatures were measured by infrared (IR) thermography (Fig. 3a and 3b) [11]. Test coupons laminated to a total thickness of 200 µm were evaluated and secured using polyimide (PI) tape.

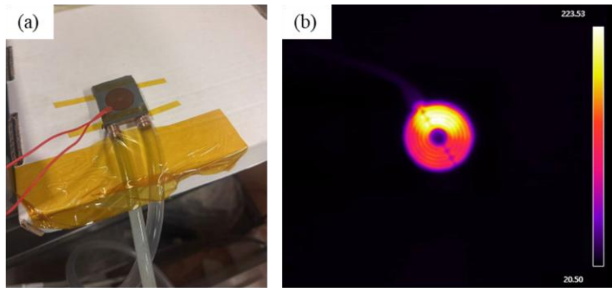

Fig. 3 Setting of steady state test for thermal performance of HTCSR with sample alone. (a) A water-cooled copper heat sink and a constant-power copper coil heater and (b) top view through IR thermography.

For finite element model, a heat source (25 mm diameter, 0.2 mm thickness) was thermally coupled to a copper cold plate (k = 400 W/(m·K)) through a 20 µm-thick TIM of the same diameter. The simulation geometry and material parameters matched those used experimentally.

All material interfaces were assigned thermal contact resistance to account for imperfect interfacial heat transfer. A representative interfacial resistance of 4.3×10^{-3} W/(mm²·K) was used based on reported micro-thermography measurements for TIM and metal interfaces [12].

C. Insulation Reliability Assessment of Solder Resist

To evaluate insulation reliability, a b-HAST was performed using substrates coated with SR. A substrate with fine-pitch comb-shaped wiring patterns (L/S = 20/20 µm) was used (Fig. 4). The test conditions were as follows: SR thickness, 20 µm; temperature, 130 °C; relative humidity, 85% RH; test duration, 200 h; bias voltage, 5 V DC. Four samples were tested for each SR. Failure was defined as an insulation resistance below 1.0×10^6 Ω.

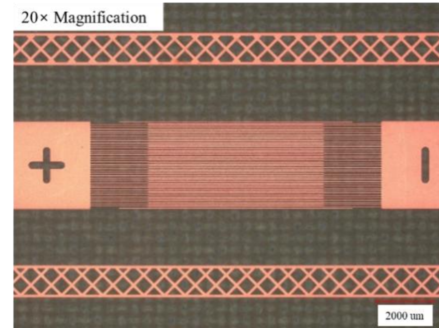

Fig. 4 The substrate for reliability test with the copper pattern (L/S = 20/20 µm).

III. Results and Discussion

A. Process Compatibility Assessments as a solder resist

First, the melt viscosity values of dry-film SRs with different filler contents were measured by a rheometer, as a result, the HTCSR of 1.2 W/(m·K) showed a melt-viscosity curve similar to that of the packaging-grade reference SR up to 120 °C (Fig. 5). Typically, dry-film SR is laminated at temperatures below 120 °C to avoid thermal effects, so that the difference of these samples does not deteriorate process compatibility, such as embeddability. On the other hand, the melt viscosity of the HTCSR with higher thermal conductivity than 1.2 W/(m·K) increased as the filler content rose. A lowest melt viscosity exceeding 100 Pa·s may adversely affect embeddability when laminating at temperatures below 100 °C to minimize thermal effects on the dry-film SR. Therefore, samples with thermal conductivity of 1.2 W/(m·K) or lower which have lower melt viscosity than 100 Pa·s were evaluated in this study.

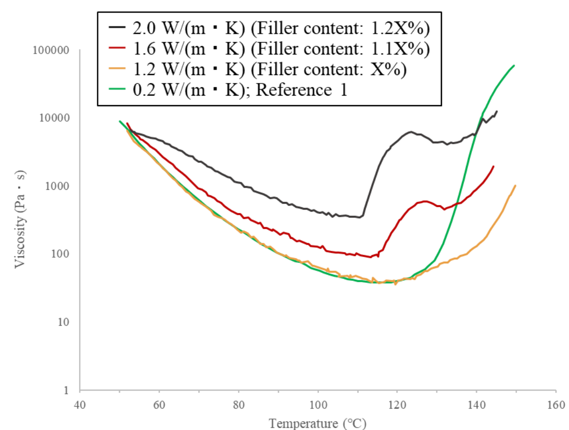

Fig. 5 The melt viscosity of dry film samples with their thermal conductivity and relative ratio of filler content. Reference is a sample used for packaging grade.

Next, the embeddability of the dry-film HTCSR of 1.2 W/(m·K) was confirmed by vacuum lamination onto a substrate with copper patterns (L/S = 20/20 μm) at 110 °C (Fig. 6). The cross-sectional image showed that the SR surface exhibited no visible topography or voids at the copper edges and the patterns were completely filled with SR, with no voids.

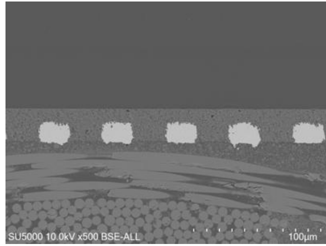

Fig. 6 Cross sectional SEM image of the substrate after lamination of HTCSR-2 (1.2 W/(m·K)) of 20 μm dry film thickness on the copper pattern (L/S = 20/20 μm).

For the HTCSR of 1.2 W/(m·K), a target opening diameter of 100 μm was achieved (Fig. 7). The opening diameters were 105/99/103 μm at the top/middle/bottom, respectively. No residue was observed on the CCL surface after development.

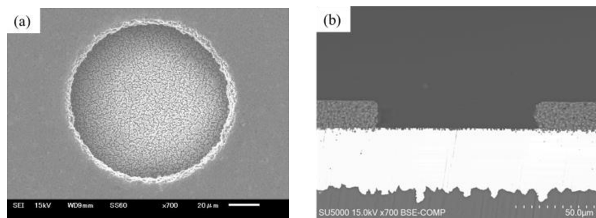

Fig. 7 (a) Top view and (b) cross-sectional SEM images of HTCSR after an exposure of 85 mJ/cm^2 and development in 1wt% Na_2CO_3aq.

Fig. 8 shows the roughness value Sa (μm) of the HTCSR after curing is as low as the value of reference 1 (for package), which is measured by a 3D profilometer (Keyence, VK-X3000). Through the design of the composition and dry-film processing, the surface roughness (Sa) achieved is about one-tenth that of liquid-type thermally conductive SRs and comparable to general-purpose package SRs. In principle, larger heat-dissipating filler particles are advantageous for increasing thermal conductivity, whereas using smaller particles improves surface smoothness but limits conductivity. Our approach mitigates this trade-off while maintaining a smooth surface.

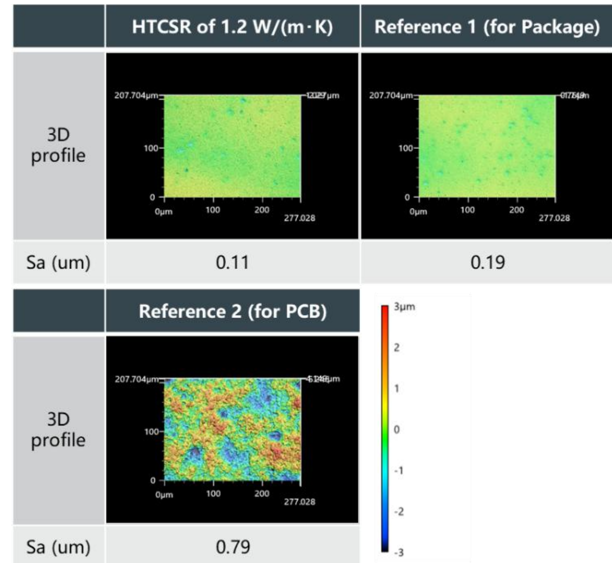

Fig. 8 3D profile images and Sa values of HTCSR of 1.2 W/(m·K), reference 1(dry film SR for package substrate) and reference 2 (liquid SR for PCB substrate of 2.0 W/(m·K)). Each samples' SR thickness is 20 μm.

B. Thermal Characterization

The equilibrium temperature at a 5 W input was 113 °C for the reference SR for the package and 72 °C for the HTCSR of 1.0 W/(m·K) (HTCSR-2), confirming a temperature reduction of 41 °C (Fig. 9). Higher thermal conductivity leads to a lower equilibrium temperature and can keep the operating temperature below the SRs' glass transition temperature, T_g (≈ 140 °C) at higher applied power. Conversely, film softening above T_g reduces interfacial contact and heat dissipation, increasing the equilibrium temperature.

The simulated temperature profiles showed good agreement with experimental measurements, with deviations within 10 °C (Fig. 9a, b). The slightly higher experimental temperatures are attributed to interfacial thermal resistances among TIMs, thermal paste, and the heat sink, which were not fully resolved in the model.

The simulations further indicate that HTCSR-2 significantly improved thermal performance, reducing the maximum junction temperature from 113.8 °C to 65.7 °C and lowering the junction-to-ambient thermal resistance from 15.7 °C/W to 8.7 °C/W compared with the FR-4 reference. These reductions confirm the superior heat-dissipation capability of the composite under high-power operation.

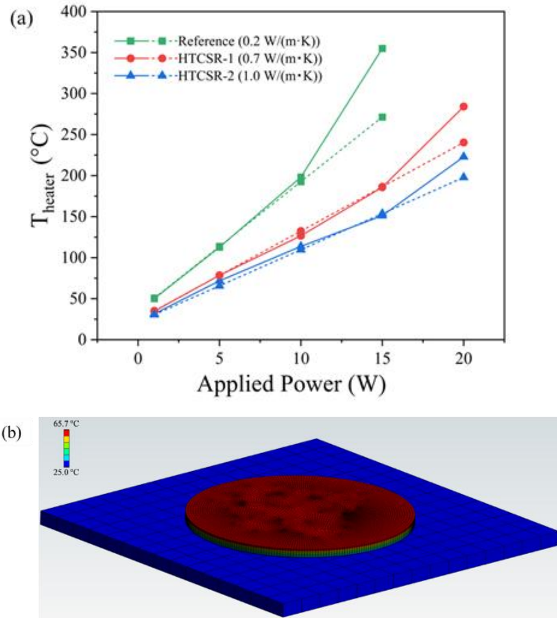

Fig. 9 (a) The results of steady state test for thermal performance of HTCSR with sample alone. The thermal conductivity of HTCSR-1, HTCSR-2 and reference sample are 0.7, 1.0 and 0.2 W/m·K, respectively. (b) temperature distribution of the SRs evaluation system at thermal equilibrium for HTCSR-2 under an applied power of 5 W, obtained from finite element analysis simulations.

C. Insulation Reliability

To evaluate insulation reliability, b-HAST testing was conducted. The results for HTCSR of 1.2 W/(m·K) and reference 1 are compared in Fig. 10. HTCSR demonstrated equivalent insulation reliability to the reference, with its insulation resistance value never falling below 1.0×10^6 Ω even after 200 hours of operation.

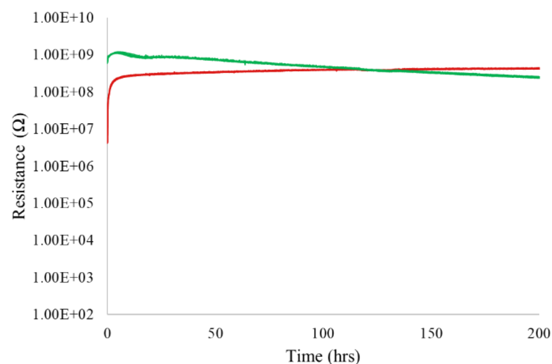

Fig. 10 Insulation reliability test of HTCSR (red, n = 4) and reference (green, n = 4) with the pattern of L/S = 20/20 μm under b-HAST condition (130 °C, 85% RH, 5V).

IV. Conclusions

We introduced a photosensitive dry-film HTCSR tailored for IC-Substrate integration, delivering isotropic thermal conductivity of 1.2 W/(m·K) at 20 μm thickness while preserving manufacturability, including a reference-like melt-viscosity window to 120 °C, void-free vacuum-lamination gap filling on L/S = 20/20 μm Cu patterns, low cured-surface roughness, and 100-μm opening patterning within a standard lamination-exposure-alkaline development-thermal cure process. Insulation reliability remained comparable to a packaging-grade SR under b-HAST (130 °C/85% RH/5 V, 200 h), with insulation resistance consistency > 1.0×10^6 Ω. Critically, steady-state thermal benchmarking on a controlled test vehicle comfirmed that replacing only the SR with an HTCSR of k = 1.0 W/m·K reduces the equilibrium temperature by 41 °C at 5 W compared to a general SR, with IR thermography indicating both enhanced lateral spreading and a lower through-plane thermal gradient across the SR layer. These results establish the HTCSR as a practical, process-compatible lever for substate-side thermal management in compact modules, enabling thermal gains without added stack up complexity. Future work will extend the evaluation to transient thermal transient thermal response, power-cycling reliability, and fine-feature patterning limits, and will investigate integration in high-power edge/AL assemblies where then, thermal capable SRs can materially impact system impact system thermal budgets.

Acknowledgment

This work was supported by the Georgia Institute of Technology 3D Systems Packaging Research Center (GT-PRC). The authors would like to thank GT-PRC members and their consortium for their cooperation in this work. The authors would like to thank Yudong Wang, Charles A Turgeon, Christopher P White and Lila D Dahal for supporting the fabrication experiments. Additionally, the authors would like to thank Dr. D. Shangguan of Thermal Engineering Associates (TEA) as a creator of TTC.

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